REMARKS

Claims 1-23 are pending in the application. Claim 2 is amended herein to overcome an informality as suggested by the Examiner. Reconsideration of the application is respectfully requested in view of the comments below.

I. REJECTION OF CLAIMS 1, 6-7, 10-13, and 15-18 UNDER 35 U.S.C. § 102(b)

Claims 1, 6-7, 10-13, and 15-18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Traynor (U. S. 6,008,659). Withdrawal of this rejection is requested for at least the following reasons.

i. Claim 1 recites determining a desired data retention lifetime for the memory cells of the ferroelectric memory device, which is not taught by Traynor.

The Office Action references Column 6, lines 3-7 of the Traynor reference as teaching the above claim language. However, this reference only teaches matching time and temperature stress to be applied to a pair of ferroelectric capacitors (76 and 78) with "performance of the capacitors" (Column 6, lines 2-3). For example, the cited reference states, "if the capacitors have short imprint performance, a short time duration and small or no temperature elevation should be used". (Column 6, lines 3-5). Selecting time and temperature stress ***according to capacitor performance*** is different than ***determining a desired data retention lifetime***, as recited in claim 1.

ii. Claim 1 recites selecting a time parameter and a temperature parameter and selecting a particular initial state according to the desired data retention lifetime, which is not taught by Traynor.

Traynor does not teach selecting time and temperatures parameter according to a *desired* data retention lifetime, but instead selects time and temperature parameters according to *imprint performance* of the ferroelectric capacitors. (Column 6, lines 1-7). In fact, Traynor merely characterizes retention performance of a pair of ferroelectric memory cells. (Column 8, lines 1-6). Similarly, Traynor also fails to teach selecting a particular initial state *according to the desired data retention lifetime*, as recited in claim

1. The portion of Traynor cited in the Office Action (*e.g.*, Column 5, lines 58-65) merely states that two ferroelectric capacitors are programmed to initial, complementary data states (*e.g.*, the first capacitor written to an "up" polarization, and the second capacitor written to "down" polarization state). The capacitors are then subjected to a stress, wherein the amount of stress (time and temperature) is a function of the imprint performance thereof. Such complementary programming of the capacitors is not a selection of a particular data state according to a desired retention lifetime as recited in claim 1.

Traynor does teach initializing the ferroelectric capacitors to an initial data state prior to the complementary programming (*see*, *e.g.*, Column 5, lines 49-56), however, the cited art specifically states that the initial data state is unimportant (stating, "[a]ny valid data state will suffice.") Clearly then, the cited art fails to teach or suggest selecting ***a particular initial state according to the desired data retention lifetime*** as claimed.

Therefore Traynor fails to anticipate the invention of claim 1. Claims 6-7, 10-13, and 15-16 depend from claim 1, and are not taught by Traynor for at least the above reasons. Accordingly, withdrawal of the rejection is respectfully requested.

iii. Claim 17 recites selecting a desired data retention lifetime for the memory cells of the ferroelectric memory device, which is not taught by Traynor.

The Office Action references Column 6, lines 3-7 of the cited art as teaching the above claim language. However, this reference, as stated above, only teaches matching time and temperature stress to be applied to a pair of ferroelectric capacitors (76 and 78) with "performance of the capacitors" (Column 6, lines 2-3).

iv. Traynor does not teach selecting one or more bake parameters according to the desired data retention lifetime and the tested data retention lifetime, as recited in claim 17.

Claim 17 comprises performing data retention lifetime testing on the ferroelectric memory device to obtain a tested data retention lifetime. ***The tested data retention lifetime is then compared to a desired data retention lifetime, and one or more bake parameters are then selected according to the comparison.*** The ferroelectric memory device is then baked according to the selected bake parameters. Traynor does not teach this feature. Rather, the cited art teaches baking the ferroelectric devices based on an identified imprint performance, wherein poorly performing devices are baked for a shorter duration than higher performing devices. ***No comparison between an actual and desired data retention lifetime is made and the consequently the bake parameters are not selected based thereon as claimed.*** Consequently, the cited art fails to anticipate the invention of claim 17.

Claim 18 depends on claim 17 and is not anticipated by Traynor for at least the above reasons. Additionally, claim 18 recites verifying the data retention lifetime after baking the ferroelectric memory device, and such feature is not taught by the cited art. Accordingly, withdrawal of the rejection of claim 17 and its associated depending claims is respectfully requested.

II. REJECTION OF CLAIMS 2-5, 8, 9, 14 and 19-23 UNDER 35 U.S.C. § 103(a)

Claims 2-5, 8, 9, 14 and 19-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Traynor (U. S. 6,008,659) in view of Kammerdiner et al. (U. S. 5,969,935) and Mitra et al. (U.S. 5,661,730). Withdrawal of this rejection is requested for at least the following reasons.

Claims 2-5, 8, 9, and 14 depend from claim 1, which Applicants have shown is not taught by Traynor. Kammerdiner et al. and Mitra et al. fail to cure the deficiencies of Traynor and are, therefore, patentable over Traynor in view of Kammerdiner et al. and Mitra et al.

Regarding claims 4-5, the Office action states that claims 4-5 are obvious because the selection of data retention lifetimes at different temperatures is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species as suggested by Mitra et al. (Column 7, lines 41-43). With respect to claims 4 and 5, Applicants respectfully disagree. Selection of desired data retention lifetimes within these claims is not a matter of "testing", but a result attainable by claims 4 and 5 and not attainable by Traynor, Kammerdiner et al., and Mitra et al. The selection of a time parameter, a temperature parameter, and an initial state are all according to the determined desired data retention lifetime. Accordingly, Traynor, Kammerdiner et al., and Mitra et al., alone or in combination, fail to teach claims 4-5.

Claim 19 depend from claim 17, which Applicants have shown is not taught by Traynor. Kammerdiner et al. and Mitra et al. fail to cure the deficiencies of Traynor. As a result, claim 19 is patentable over Traynor in view of Kammerdiner et al. and Mitra et al.

Claim 20 is rejected in the Office Action, however no explanation of this rejection is provided.

i. ***Claim 20 recites adjusting the process time and the process temperature according to the obtained tested data retention lifetime and a suitable data retention lifetime, wherein the process time and the process temperature are selected to selectively improve data retention of the memory device.***

Traynor, Kammerdiner et al, and Mitra et al., alone or in combination, do not teach adjusting the process time and the process temperature to selectively improve data retention as recited in claim 20. Traynor fails to teach adjusting the process time and the process temperature and only characterizes retention performance of a pair of ferroelectric memory cells. (Column 8, lines 1-6). Kammerdiner et al. teach improving retention performance by a careful selection of ferroelectric constituent elements (Column 7, lines 33-37) and do not teach adjusting process time and process

temperature to improve data retention. Mitra et al. also fail to teach adjusting process time and process temperature to improve data retention and instead selects time and temperature according to ferroelectric materials employed (Column 4, lines 23-26).

Claims 21-23 depend from claim 20, which Applicants have shown is not taught by Traynor. Kammerdiner et al. and Mitra et al., alone or in combination.

Accordingly, it is respectfully requested that this rejection of claims 2-5, 8, 9, 14 and 19-23 be removed.

III. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-35492.

Respectfully submitted,
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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper or item referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first-class mail in an envelope addressed to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: May 19, 2004 Christine Gillroy
Christine Gillroy